On the control of input–constrained boost DC–to–DC power converters ⋆

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Abstract. Boost DC–to–DC (direct current–to–direct current) power converters are useful in many applications as part of devices used at home and industry. The theoretical and practical study of boost DC–to–DC power converters has prompted the attention of many researchers. In this paper, a new controller for Boost DC–to–DC power converters is proposed. The new scheme takes into account that the duty cycle is constrained to physically admissible values. The analysis of the closed–loop trajectories provides the conclusion that output voltage regulation is achieved in asymptotic form. Our theoretical results are supported by using numerical simulations and real–time experiments.

1 Introduction

The problem of regulating the output voltage of a boost DC–to–DC (direct current–to–direct current) power converter has attracted the attention of many control researchers for several years now. Besides its practical relevance, the system is an interesting theoretical case study because it is a switched device whose averaged dynamics are described by a bilinear second order non–minimum phase system with saturated input [1].

In order to provide a degree of robustness to compensate uncertainties in the load, supply voltage and unmodeled disturbances, many control algorithms have devised to achieve voltage output regulation.

A brief literature review is provided in the next. In the textbooks [2] and [3] a number of algorithms for the boost DC–to–DC power converter are analyzed, but none of them deals with the practical situation that the duty cycle input should be into admissible values. The work of Spinetti, Fossas and Biel in [4] presented an interesting controller which requires feedback of the inductor current and output voltage. The scheme proposed there provides a very fast convergence of the output voltage to the desired one. However, two main disadvantages are detected in this controller: the assumption that all the boost parameters should be known and the assumption that the control input may take any real value, which is not possible in practice. In the paper by Karagiannis,

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Astolfi and Ortega in [5] proposed an algorithm that leaves aside the inductor current feedback. A certain degree of robustness is provided thanks to adaptation of the supply voltage. Other advantage of this scheme is that stability is guaranteed even if duty cycle saturation occurs.

In spite of the fact that the algorithms proposed in the literature achieve the control objective, only a few of them takes into account the practical limitation that the percentage of duty cycle $u(t)$ is limited to

$$u(t) \in [0, 1). \tag{1}$$

In other words, no much attention has been devoted to design control schemes that guarantee output voltage regulation of a input–saturated boost converter. See for instance the work in [5].

In this paper, a new controller is proposed. The new scheme takes into account the physical constraint that the duty cycle input $u(t)$ should satisfy (1). The analysis of the closed–loop trajectories provides the conclusion that output voltage regulation is achieved in asymptotic form. Our theoretical results are supported by using numerical simulations and real–time experiments.

In ideal conditions (assuming that all the boost DC–to–DC converter parameters are known and that there are not disturbances) the new scheme guarantees global convergence of the output voltage to the desired one, while the generated duty cycle control input stays into the practical admissible limits.

Although in presence of model disturbances, the algorithm is not able to achieve output voltage regulation, which is corroborated by simulation and experiment, the proposed methodology is promising since several extensions can be developed to improve its performance and robustness.

The present document is organized as follows. Section 2 deal with the boost DC–to–DC dynamic model. The new scheme and the analysis of the closed–loop trajectories are presented in Section 3. Section 4 is devoted to numerical tests, while Section 5 is concerned to real–time experimental results. Finally, some concluding comments are drawn is Section 6.

2 Boost DC–to–DC converter model and control goal

2.1 Boost DC–to–DC model converter

Consider the switch–regulated boost converter circuit of Figure 1. The positive quantity E represents the external voltage supply, $i(t)$ is the current through inductor $L > 0$, $v(t)$ is the voltage through capacitor C, and R the load resistor. The signal u_s takes values in the discrete set $\{0, 1\}$.

In order to represent this switch–regulated circuit, the following average non–linear equation system can be obtained using circuit analysis via Kirchhoff laws

$$L\frac{di}{dt} = -[1-u]v + E, \tag{2}$$

$$C\frac{dv}{dt} = [1-u]i - \frac{v}{R}, \tag{3}$$

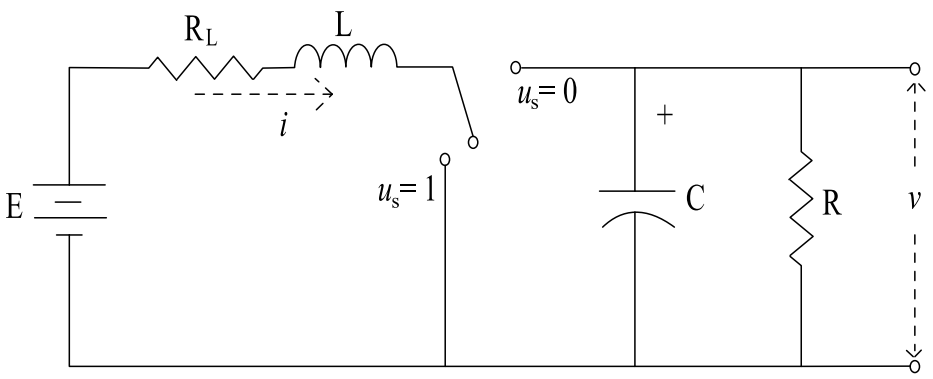

Fig. 1. The boost converter circuit.

where $u(t)$ is a continuous control signal representing the duty cycle percentage of the PWM circuit controlling the switch. See the textbooks [2] and [3] for further details in the modeling of the boost DC–to–DC converter.

2.2 Control goal

It is easy to show that an equilibrium point of the system (2)–(3), assuming a constant duty cycle percentage $u(t) = u_e$, is given by

$$i = i_d = \frac{v_d}{[1 - u_e]R},$$
$$v = v_d = \frac{E}{1 - u_e}.$$

Solving for u_e, we have

$$u_e = 1 - \frac{E}{v_d},$$

where v_d is the desired voltage. In practice, the actual duty cycle percentage $u(t)$ should satisfy

$$0 < u_e < 1,$$

therefore $v_d > E$. Notice that $u(t) = u_e = 1$ results in an undefined equilibrium point i_d and v_d.

The control goal consists in the specification of the desired output voltage $v_d > E$ and the design of a control law $u(t)$ satisfying the constraint (1) such that the output voltage achieves

$$\lim_{t \to \infty} v(t) = v_d, \tag{4}$$

while the inductor current $i(t)$ remains bounded.

3 Proposed scheme, analysis and extensions

3.1 Proposed scheme

In consideration to the control goal established above, the controller proposed in this paper is given by

$$u = 1 - sat\left(\frac{E}{V_d} + \gamma[V_d e_i - i_d e_v]\right), \tag{5}$$

where $\gamma > 0$ is a constant,

$$e_i = i - i_d, \tag{6}$$
$$e_v = v - V_d, \tag{7}$$

are the current error and voltage error, respectively, and

$$sat(z) = \begin{cases} 1 - \xi_m, \text{ if } z < \xi_m, \\ 1 - z, \text{ if } \xi_m \leq z \leq \xi_M, \\ 1 - \xi_M, \text{ if } z > \xi_M, \end{cases} \tag{8}$$

with

$$0 < \xi_m < \xi_M < 1.$$

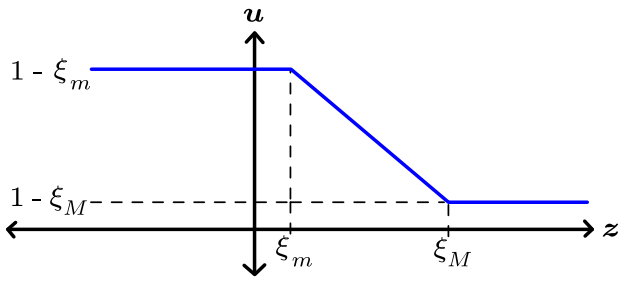

Fig. 2. Profile of the function $sat(z)$.

The profile of the saturation function $sat(z)$ in (8) is depicted in Figure 2. It is worthwhile to notice that by using the definition of the saturation function (8), it is possible to show that the duty cycle percentage $u(t)$ satisfies the following inequality

$$1 - \xi_M \leq u(t) \leq 1 - \xi_m.$$

Therefore, the constraint (1) is satisfied for all $t \geq 0$.

It is noteworthy that the number ξ_m and ξ_M are chosen so that

$$u = 1 - sat\left(\frac{E}{V_d}\right) = 1 - \frac{E}{V_d} = u_e,$$

which is always satisfied for

$$0 < \xi_m \leq \frac{E}{v_d} \leq \xi_M < 1. \tag{9}$$

3.2 Analysis

Let us define

$$x = v_d e_i - i_d e_v \tag{10}$$

in order to simplify the notation.

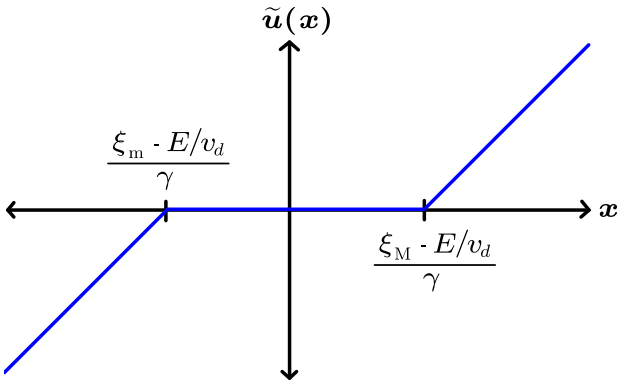

Fig. 3. Profile of the function $\tilde{u}(x)$.

Substituting (6)–(7) and the duty cycle percentage input $u(t)$ in (5) into the boost converter dynamics (2)–(3), the closed–loop system can be written as

$$L\frac{de_i}{dt} = -\gamma x[e_v + v_d] + \tilde{u}(x)[e_v + v_d] - \frac{E}{v_d}e_v, \tag{11}$$

$$C\frac{de_v}{dt} = \gamma x[e_i + i_d] - \tilde{u}(x)[e_i + i_d] + \frac{E}{v_d}e_i - \frac{1}{R}e_v, \tag{12}$$

where

$$\tilde{u}(x) = \frac{E}{v_d} + \gamma x - sat\left(\frac{E}{v_d} + \gamma x\right) \tag{13}$$

is a dead zone–type nonlinear function. The profile of the function $\tilde{u}(x)$ is illustrated in Figure 3. Even more, $\tilde{u}(x)$ can be explicitly given as

$$\tilde{u}(x) = \begin{cases} \frac{E}{v_d} + \gamma x - \xi_M, & \text{for } \frac{E}{v_d} + \gamma x > \xi_M, \\ 0, & \text{for } \xi_m \leq \frac{E}{v_d} + \gamma x \leq \xi_M, \\ \frac{E}{v_d} + \gamma x - \xi_m, & \text{for } \frac{E}{v_d} + \gamma x < \xi_m. \end{cases} \tag{14}$$

See Figure 3 for a plot of the function $\tilde{u}(x)$ in (14).

It is possible to show that the state space origin $[e_i\ e_v]^T = [0\ 0]^T$ is an equilibrium point of the closed–loop (11)–(12).

Now, let us introduce the following Lyapunov function candidate

$$W = \frac{1}{2}Le_i^2 + \frac{1}{2}Ce_v^2, \tag{15}$$

which is positive definite and radially unbounded. The time–derivative of W along of the closed–loop system trajectories (11)–(12) is given by

$$\dot{W} = -\gamma x^2 - \frac{e_v^2}{R} + \tilde{u}(x)x, \tag{16}$$

which is obtained after some direct algebra.

Now, in order to find a upper bound on $\dot{W}$ let us write the product $\tilde{u}(x)x$ explicitly as follows

$$\tilde{u}(x)x = \begin{cases} [\frac{E}{v_d} - \xi_M]x + \gamma x^2, & \text{for } x > \frac{\xi_M - E/v_d}{\gamma}, \\ 0, & \text{for } \frac{\xi_m - E/v_d}{\gamma} \leq x \leq \frac{\xi_M - E/v_d}{\gamma}, \\ [\frac{E}{v_d} - \xi_m]x + \gamma x^2, & \text{for } x < \frac{\xi_m - e/v_d}{\gamma}. \end{cases} \tag{17}$$

Similarly, the profile of $\tilde{u}(x)x$ is shown in Figure 4.

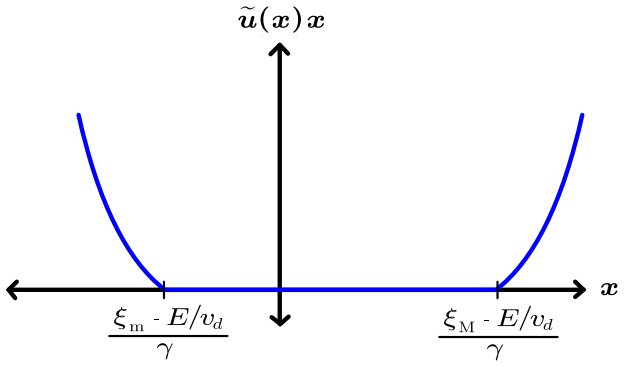

Fig. 4. Profile of the function $\tilde{u}(x)x$.

Taking into account the explicit definition of the function $\tilde{u}(x)x$ in (17), the time derivative of Lyapunov function candidate $\dot{W}$ in (16) can be expressed as

$$\dot{W} = \begin{cases} [\frac{E}{v_d} - \xi_M]x - \frac{e_v^2}{R}, & \text{for } x > \frac{\xi_M - E/v_d}{\gamma}, \\ -\gamma x^2 - \frac{e_v^2}{R}, & \text{for } \frac{\xi_m - E/v_d}{\gamma} \leq x \leq \frac{\xi_M - E/v_d}{\gamma}, \\ [\frac{E}{v_d} - \xi_m]x - \frac{e_v^2}{R}, & \text{for } x < \frac{\xi_m - E/v_d}{\gamma}, \end{cases} \tag{18}$$

Notice that in the sector $x > \frac{\xi_M - E/v_d}{\gamma}$, where $x > 0$, the inequality

$$[\frac{E}{v_d} - \xi_M]x < 0$$

is accomplished because condition (9). Therefore, $\dot{W} = [\frac{E}{v_d} - \xi_M]x - \frac{e_v^2}{R} \leq -\frac{e_v^2}{R}$. Proceeding in a similar form in the other two sectors, it is possible to show that a upper bound of $\dot{W}$ in (18) is given by

$$\dot{W} \leq -\frac{e_v^2}{R}, \ \forall \ \begin{bmatrix} e_i \\ e_v \end{bmatrix} \in \mathbb{R}^2, \tag{19}$$

which is globally negative semidefinite, and implies that the state space origin $[e_i \ e_v]^T = [0 \ 0]^T$ is stable in the Lyapunov sense [6]. Besides, W in (15) is a Lyapunov function of the system (11)–(12)

Finally, since the system (11)–(12) is autonomous, by invoking LaSalle's theorem, the proof that the state space origin $[e_i \ e_v]^T = [0 \ 0]^T$ is globally asymptotically stable can be achieved. Then,

$$\lim_{t \to \infty} \begin{bmatrix} e_i(t) \\ e_v(t) \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \end{bmatrix}, \tag{20}$$

and the control goal (4) is satisfied.

4 Numerical simulations

In order to illustrate the above analysis, simulations have been carried out assuming that the boost converter is a continuous system and the controller $u(t)$ in (5) is implemented in discrete time with a sample time $T_s = 0.0001$ [s], which produces a sampled–data system.

The following values were chosen: $L = 5$ [mH], $C = 12$ [μF] and $R = 182$ [Ω]. Besides, we selected $\xi_m = 0.1$, $\xi_M = 0.9$ and $\gamma = 0.1$.

The initial conditions of the system were

$$i(0) = 0.0598 \text{ [A] and } v(0) = 9.7440 \text{ [V]}. \tag{21}$$

We carried out a simulation with a duration of 0.01 [s], specifying a desired voltage v_d = 15 $[V]$. The results are observed in Figure 5, where the time evolution of the output voltage $v(t)$, the inductor current $i(t)$ and the duty cycle percentage $u(t)$ are appreciated. The capacitor voltage $v(t)$ reach v_d in approximately 0.003 [s], enough time for $u(t)$ to reach a practically constant value.

Now, results shown in Figure 6, consider that $v_d(t)$ is a square periodic signal defined as

$$v_d(t) = \begin{cases} 15 \text{ [V]}, & \text{for } 0 \leq t \leq 0.5T_r, \\ 20 \text{ [V]}, & \text{for } 0.5T_r \leq t \leq T_r, \end{cases} \tag{22}$$

with $T_r = 1.0$ [s] defining the period of v_d. In this case the simulation had a duration of 5 [s]. Similarly, Figure 6 depicts the time evolution of the output voltage $v(t)$, the inductor current $i(t)$ and the duty cycle percentage $u(t)$. It is observed that the output voltage $v(t)$ converges to v_d.

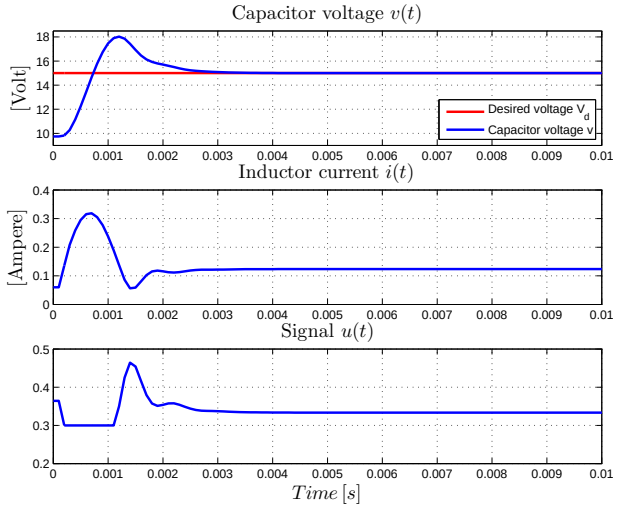

Fig. 5. Simulation: Capacitor voltage $v(t)$, inductor current $i(t)$ and control signal $u(t)$ for $0 \leq t \leq 0.01$ [s] and $v_d = 15$ [V].

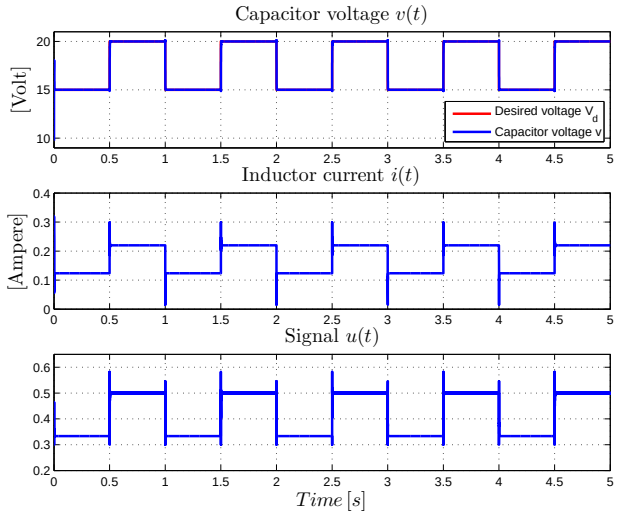

Fig. 6. Simulation: Capacitor voltage $v(t)$, inductor current $i(t)$ and control signal $u(t)$ for $0 \leq t \leq 5$ [s] and $v_d(t)$ in (22).

5 Experimental results

Laboratory experiments have taken place under similar conditions than in the numerical simulations. The switching frequency of the PWM was 50 $[kHz]$. We choose $\xi_m = 0.1$, $\xi_M = 0.9$ and γ = 0.5.

Figure 7 shows that the rise time is almost 0.1 [s], much more time than the one shown in the simulation results; compare Figure 5 with respect to Figure 7.

The control signal $u(t)$ is saturated in very short periods of time. However, there is no any operation problem since the output voltage $v(t)$ and the inductor current $i(t)$ remain bounded for all time.

We also present in Figure 8 the output voltage $v(t)$ and the inductor current $i(t)$ when $v_d(t)$ in (22) is used. Besides, Figure 8 shows also the time evolution of the control input $u(t)$.

In Figure 8 it is appreciated a steady state error of 0.35 [V] when $v_d = 15$ [V], and 0.70 [V] when $v_d = 20$ [V]. In addition to the discrete implementation of the controller, there are other model uncertainties and disturbances, such as deviations in the values of the inductance L, capacitance C and load resistance R. Besides, the inductor has a significative resistance which also causes the steady state error.

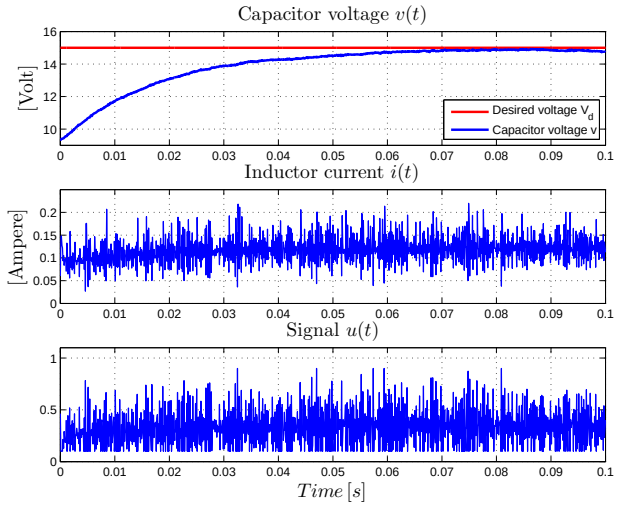

Fig. 7. Experiment: Capacitor voltage $v(t)$, inductor current $i(t)$ and control signal $u(t)$ for $0 \leq t \leq 0.01$ [s] and $v_d = 15$ [V].

6 Conclusions

A new control scheme was proposed in this paper. The new controller is based in a hard saturation function in order to keep the duty cycle percentage into admissible physical

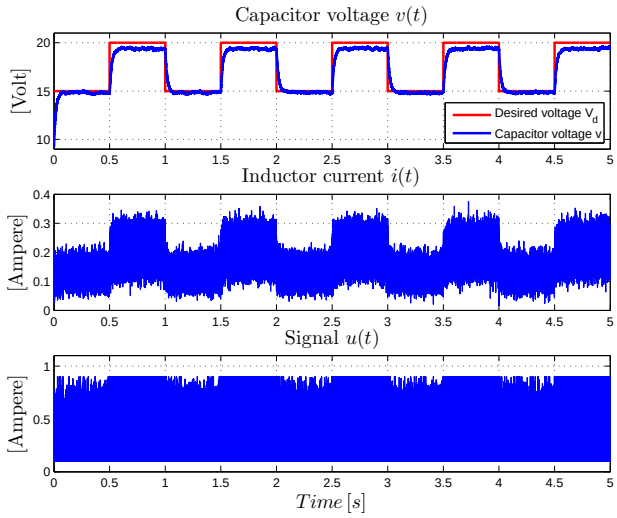

Fig. 8. Experiment: Capacitor voltage $v(t)$, inductor current $i(t)$ and control signal $u(t)$ for $0 \leq t \leq 5$ [s] and $v_d(t)$ in (22).

values. In simulation results, $v(t)$ reaches v_d, while in experimental results $v(t)$ is close to v_d. As explained before, the reason for this situation is that in experiment the system is affected by disturbances. In order to improve the performance and robustness, the introduction of a dynamic extension, such as an integral action, is being explored currently.

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